

XRT83SL34/L34EVAL EVALUATION SYSTEM USER MANUAL

EVALUATION KIT PART LIST

This kit contains the following:

- XRT83SL34/L34EVAL Application Board
- XRT83SL34/L34 GUI Evaluation Software
- XRT83SL34/L34 128-Pin TQFP
- XRT83SL34/L34EVAL User Manual
- XRT83SL34/L34 Datasheet

FEATURES

- CPLD Design Which Emulates Microprocessor Support for a Parallel Interface
- 25 DIN Connector for Easy Connection Through a Standard Parallel Port to a PC
- CD ROM or Floppy Disk Containing GUI Software (Executable File)
- Line Interface Modules Coupled to Receiver Inputs and Transmitter Outputs
- Power Supply Design Allowing a Single 3V Supply voltage
- Accessible I/O Interface for Common Laboratory Equipment
- Optimized layout with Four Layers

INTRODUCTION

XRT83SL34/L34EVAL is a complete printed circuit board for characterizing Exar's XRT83SL34/L34. XRT83SL34/L34 is a fully integrated four channel, long haul, short haul line interface unit for T1, E1 and J1 applications.

This application board combines a proven PC board layout with optimized analog and digital interface circuitry. XRT83SL34/L34EVAL contains device being tested, CPLD for emulating microprocessor support, line interface modules coupled to receiver inputs and transmitter outputs, and I/O headers for flexible user interface. Complete AC and DC performance of XRT83SL34/L34 can be evaluated by interfacing external laboratory equipment.

SYSTEM CONFIGURATION-LAB SETUP

XRT83SL34/L34EVAL application board is setup as a common test circuit. Figure 1 shows a simplified block diagram of a default test configuration.

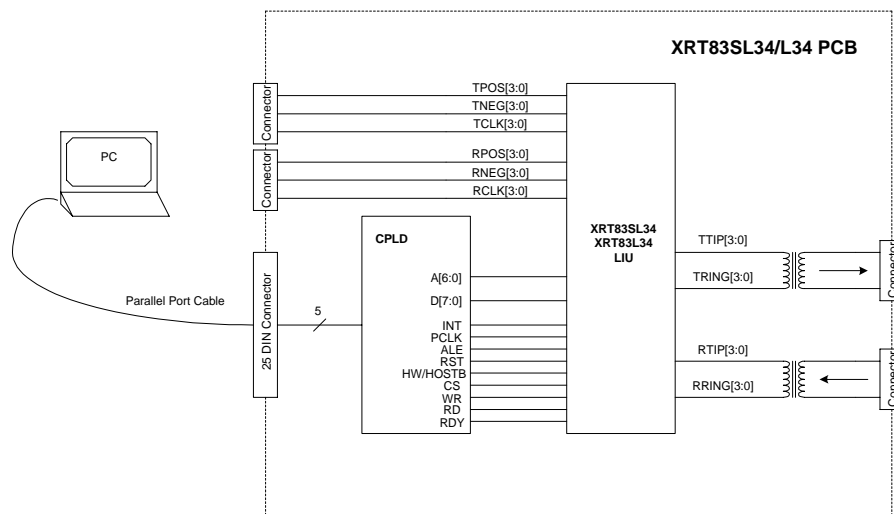


Figure 1 Simplified Block Diagram of XRT83SL34/L34EVAL Application Board

APPLICATION CIRCUITRY

CPLD

XRT83SL34/L34EVAL uses a CPLD designed to emulate a microprocessor support module. Using Exar's GUI software (included in the evaluation kit), XRT83SL34/L34EVAL can be controlled through a standard parallel port cable connected to a PC. The GUI was written to simplify evaluation of Exar's LIU. Access to all control registers and functionality of all four channels is available. For information on GUI software, see section "XRT83SL34/L34EVAL GUI SOFTWARE" of this manual. Figure 3 is a simplified block diagram of CPLD interface.

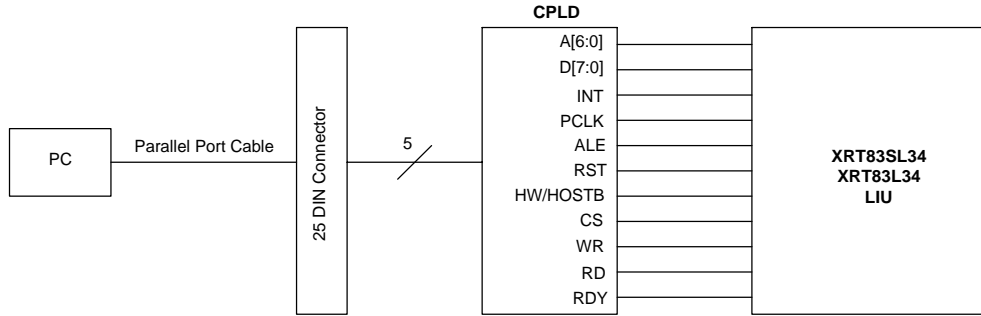


Figure 3 Simplified Block Diagram of CPLD Interface

LINE INTERFACE MODULE

Internal Impedance Mode

XRT83SL34/L34 has an internal and external impedance mode. For internal impedance mode, no termination resistors are necessary for transmitter outputs or receiver inputs. This allows one bill of materials for all three applications T1, E1, or J1. Figure 4 is a simplified block diagram of internal impedance mode. For external impedance mode, see the following sections for resistor values chosen for corresponding applications.

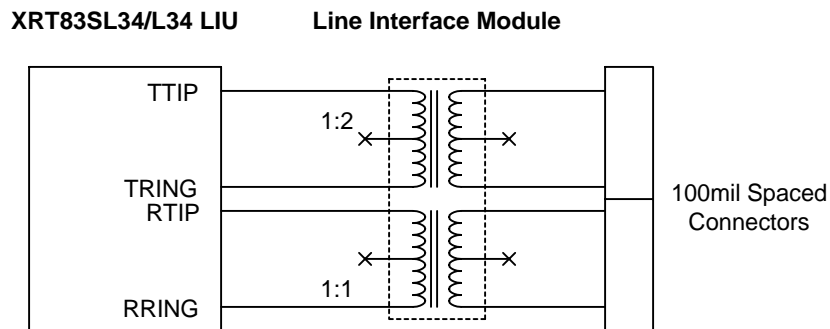


Figure 4 Simplified Block Diagram of Internal Impedance Mode

External Impedance Mode (T1/J1, 1.544MHz, 100ohm/110ohm)

XRT83SL34/L34EVAL can be programmed for external impedance mode through microprocessor interface. For T1 applications, two 3.1ohm resistors are necessary on transmitter outputs of the LIU. A 100ohm resistor is necessary on receiver inputs. (Note: These values do not change when using either a 1:2 or 1:2.45 turns ratio on transmit side) Figure 5 is a simplified block diagram of external mode for T1 applications.

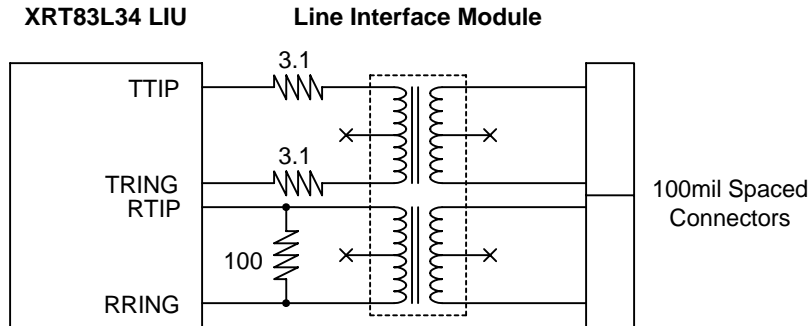


Figure 5 Simplified Block Diagram of External Mode, T1/J1

External Impedance Mode (E1, 2.048MHz, 75ohm or 120ohm)

XRT83SL34/L34EVAL can be programmed for external impedance mode through microprocessor interface. For E1 applications, two 9.1ohm resistors are necessary on transmitter outputs of the LIU. A 75ohm (75ohm termination) or 120ohm (120ohm termination) resistor is necessary on receiver inputs. (Note: Resistor values on transmit side change to 6.2ohms when using a 1:2.45 turns ratio) Figure 6 is a simplified block diagram of external mode for E1 applications.

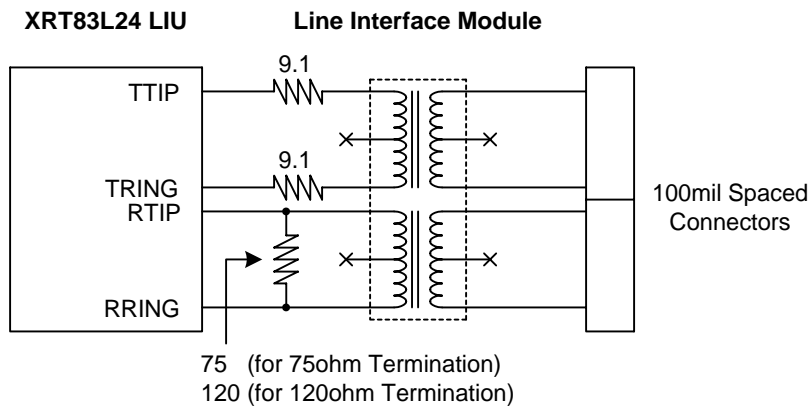


Figure 6 Simplified Block Diagram of External Mode, E1 75ohm and 120ohm

INPUT CLOCK SOURCE

Whether using T1 or E1, a variety of input clock source(s) can be configured. There are two input clock pins on XRT83SL34/L34, MCLKE1 and MCLKT1. Note: When using one clock source T1 or E1, both pins must be connected together. This can be applied on XRT83SL34/L34EVAL by shorting jumper J33. In addition to two input clock pins, an internal clock synthesizer within XRT83SL34/L34 provides more flexibility when driving the LIU. This allows for one clock source to generate T1 or E1 clock rates. For example: An 8kHz input clock can be applied to MCLKE1 as a single clock input source. Then, XRT83SL34/L34 can be configured to operate at 1.544MHz or 2.048MHz. Figure 7 is a simplified block diagram of input clock circuitry on XRT83SL34/L34EVAL. See XRT83SL34/L34 datasheet for more information regarding input clock source(s).

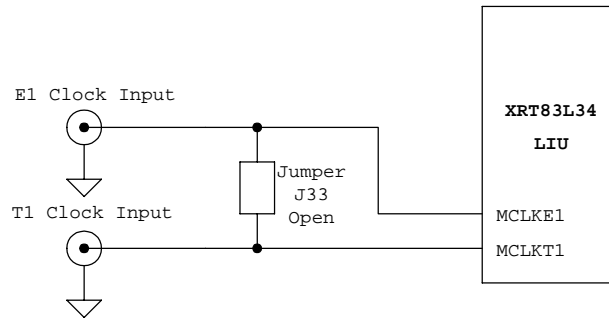
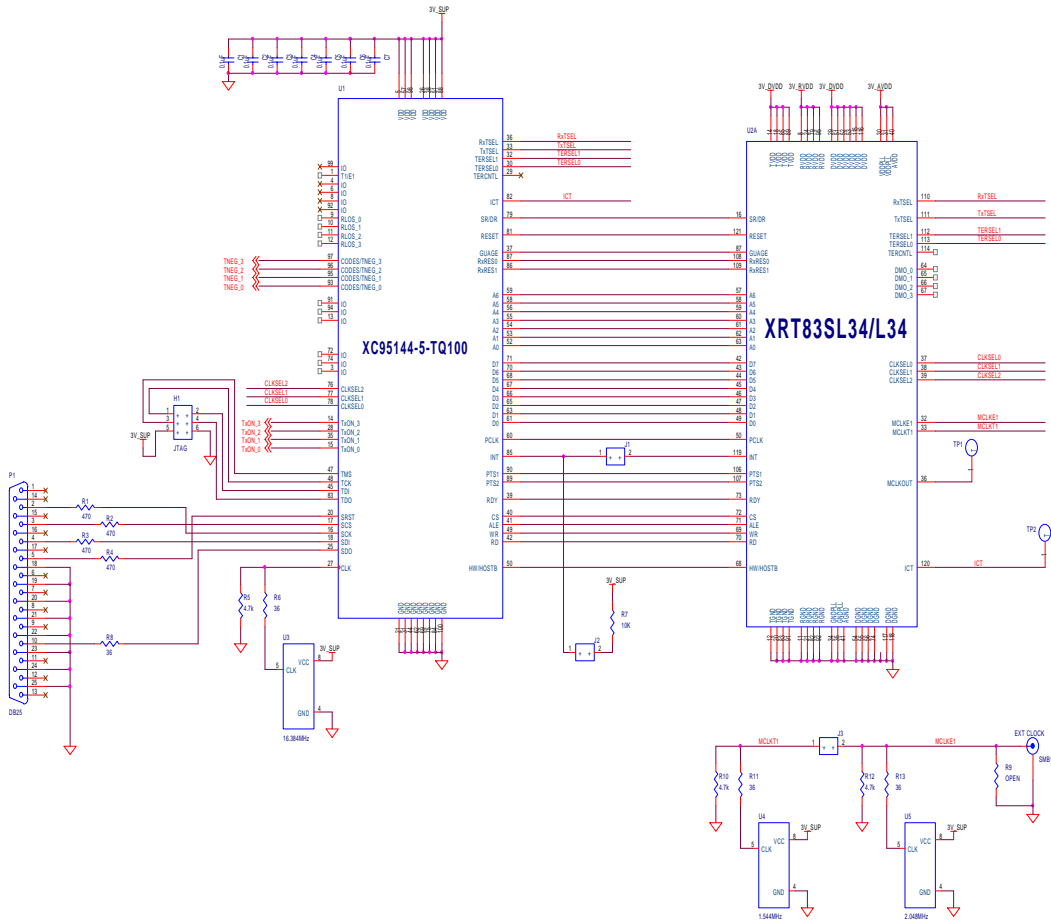


Figure 7 Simplified Block Diagram of Input Clock Source(s)

XRT83SL34/L34 LONG HAUL, SHORT HAUL LIU MAIN INTERFACE



Design File Name = H:\XRT83SL34\SCHEMATIC\XRT83SL34.DSN

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|------------------------|-------------------------------------|--------|
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| Part | XRT83SL34 | |
| Rev | Document Number | Rev |
| C | XRT83SL34-LONG HAUL, SHORT HAUL LIU | B |
| Date | Tuesday, September 12, 2006 | Page |
| | | 1 of 2 |

Figure 8 Schematic Page 1 of the XRT83SL34/L34EVAL Application Board

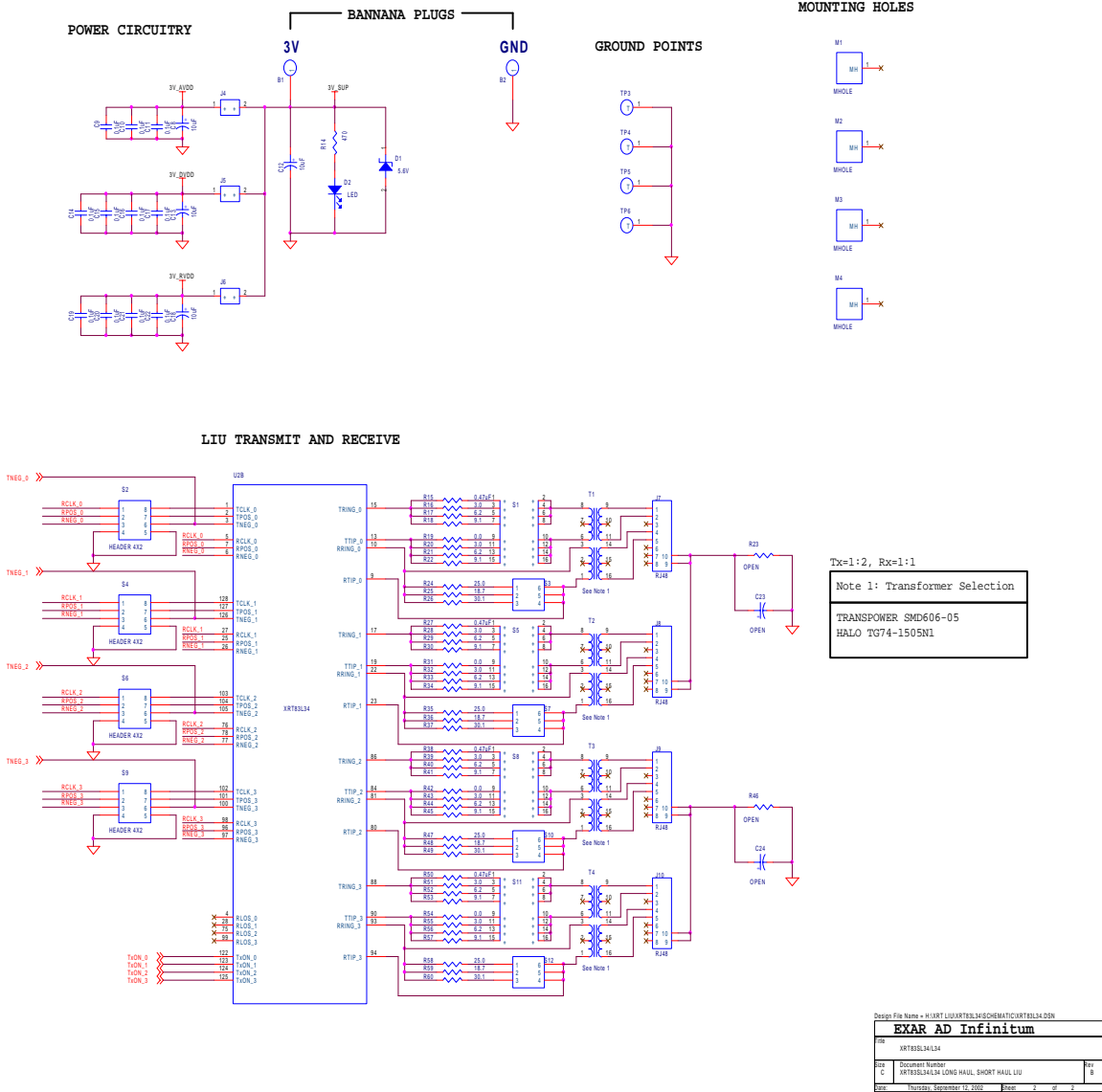


Figure 9 Schematic Page 2 of the XRT83SL34/L34EVAL Application Board

Top Silk Screen

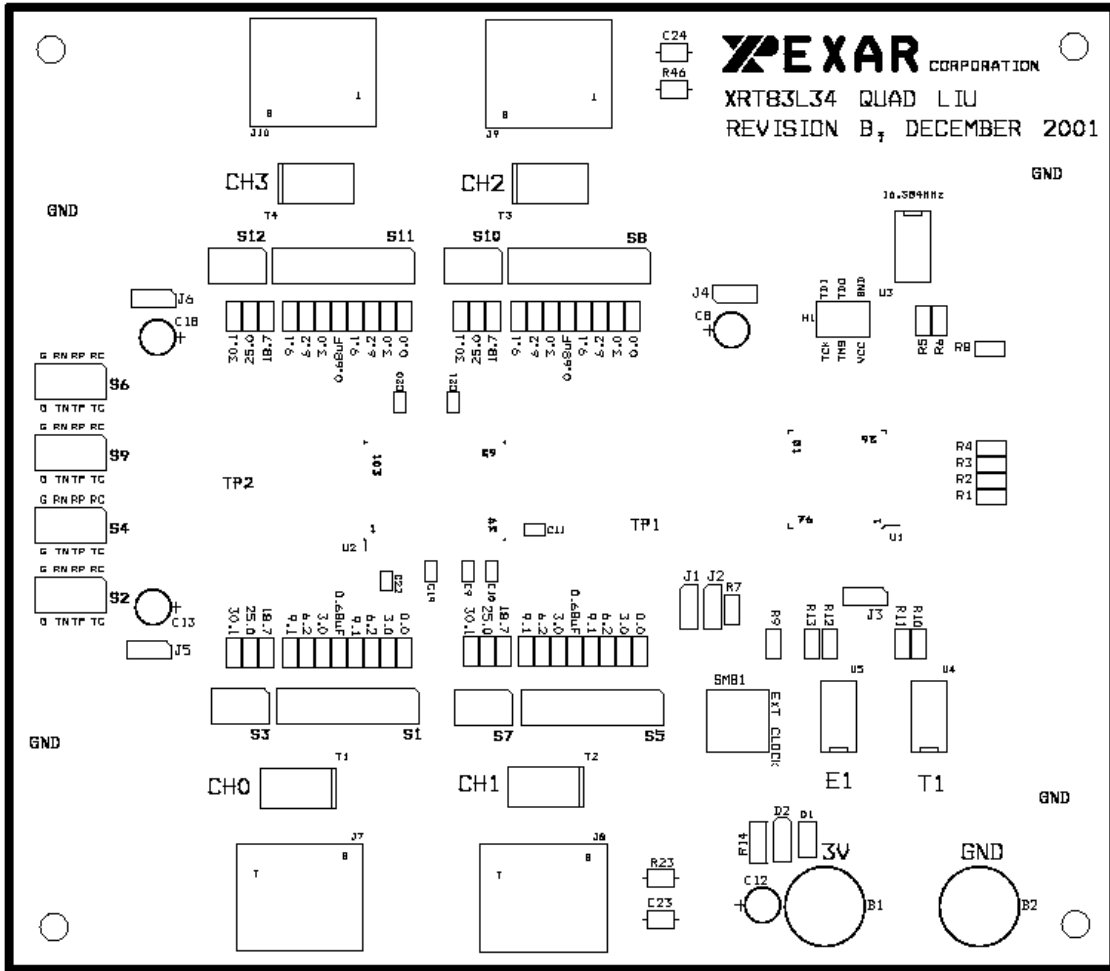


Figure 10 Layout Plot-Top Silk Screen of the XRT83SL34/L34EVAL Application Board

Top Layer

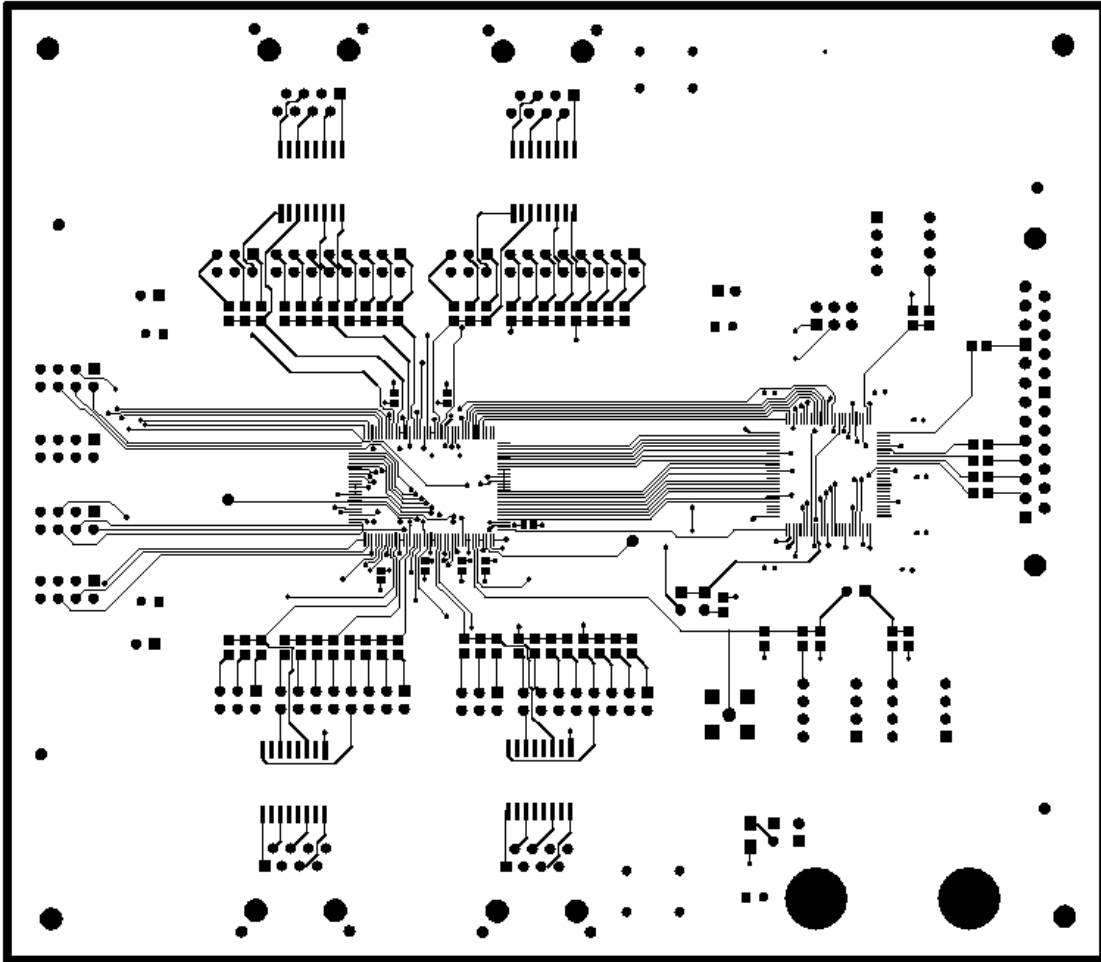


Figure 11 Layout Plot-Top Layer of the XRT83SL34/L34EVAL Application Board

Ground Plane

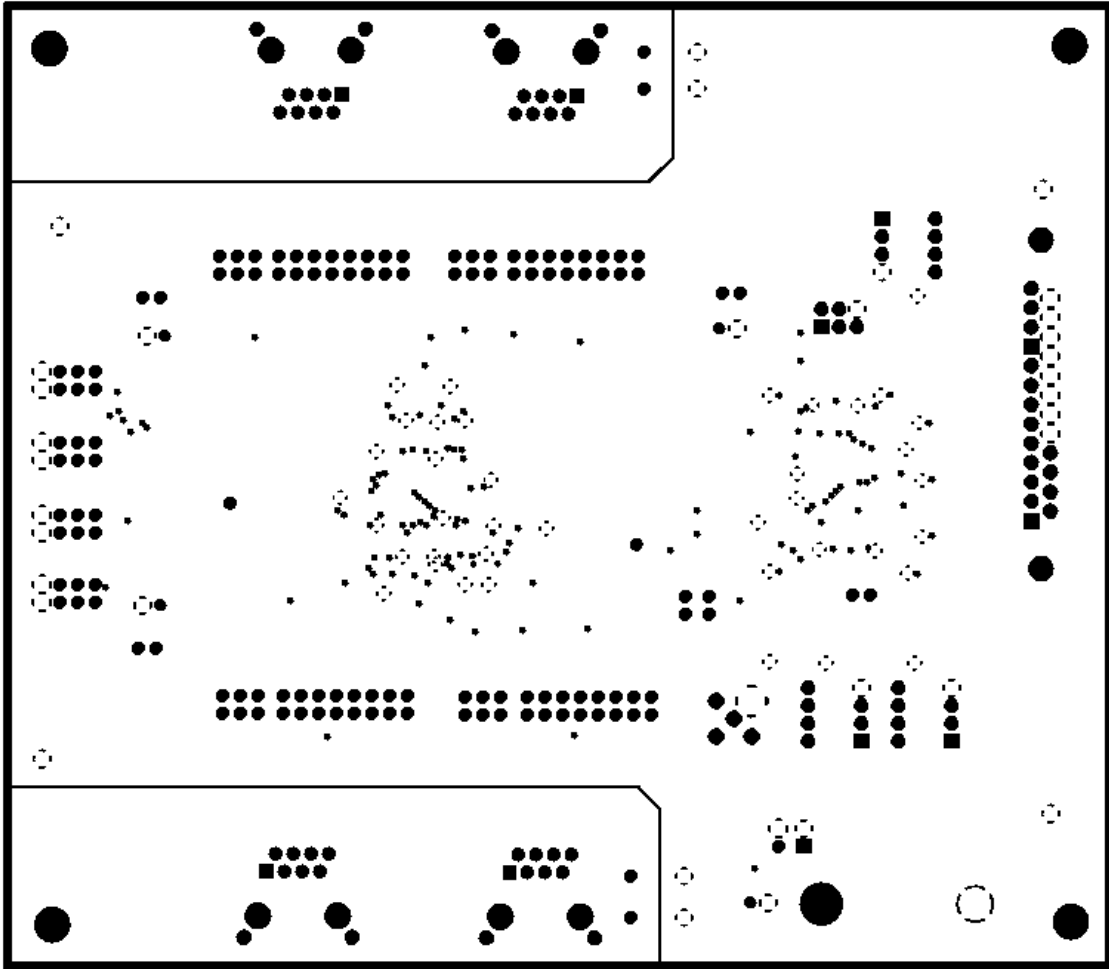


Figure 12 Layout Plot-Ground Plane of the XRT83SL34/L34EVAL Application Board

Power Plane

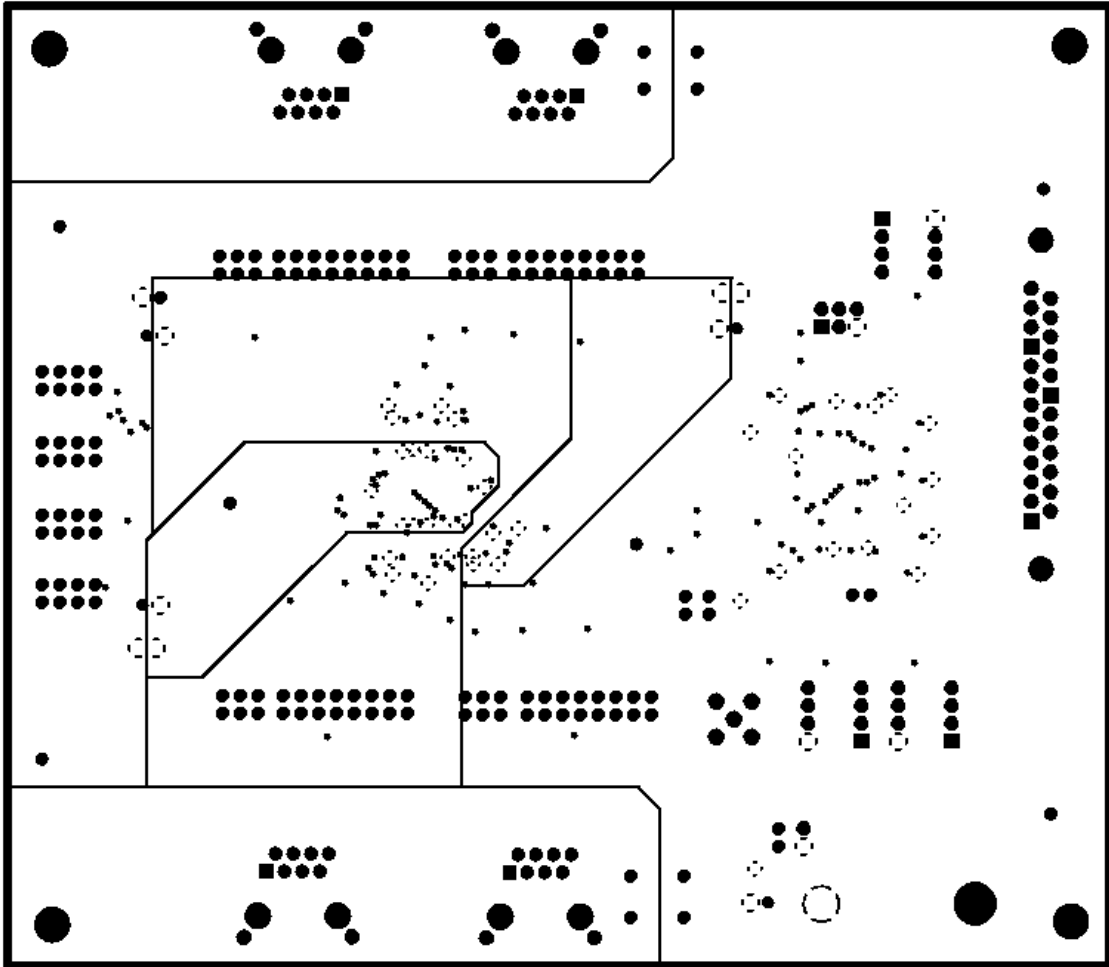


Figure 13 Layout Plot-Power Plane of the XRT83SL34/L34EVAL Application Board

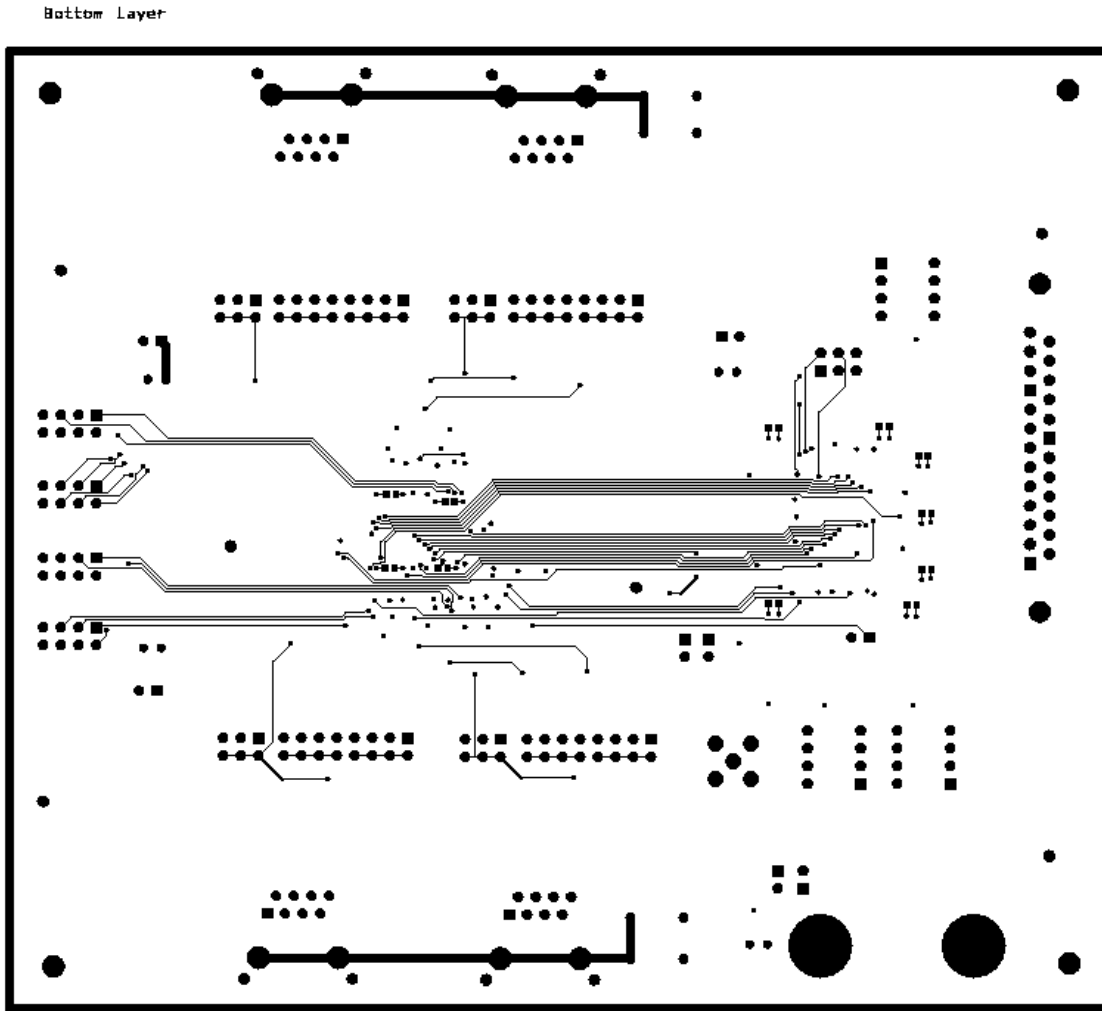


Figure 14 Layout Plot-Bottom Layer of the XRT83SL34/L34EVAL Application Board

The XRT83SL34/L34 Evaluation Board GUI Software

The XRT83SL34/L34 Evaluation Board Kit comes with a floppy disk / CD ROM that contains a file of the name: "xrt83L34vxx.exe". This file is the executable code for the "XRT83SL34/L34 Evaluation Board GUI Software".

This section provides the reader with a thorough overview of the XRT83SL34/L34 Evaluation Board GUI Software and all of its features.

Installing the XRT83SL34/L34 Evaluation Board GUI Software, on to the PC

Installing the "XRT83SL34/L34 Evaluation Board GUI Software, onto a PC is simple. The user can copy the file from the floppy disk / CD ROM onto the hard-drive of the PC (within the user's directory of choice). Then, simply double click the executable file to launch the GUI interface.

Connecting the XRT83SL34/L34 Evaluation Board to the PC

When the XRT83SL34/L34 Evaluation Board is operating in the "Host" Mode, the user will exercise command and control over the Evaluation Board via a PC which is executing the "XRT83SL34/L34 Evaluation Board GUI" Software. Prior to starting up and executing the GUI Software, the user is required to connect the parallel port connector of the Evaluation Board to the parallel-port of the PC, via a parallel-port cable. The "XRT83SL34/L34 Evaluation Board will communicate with the XRT83SL34/L34 Evaluation Board hardware via this parallel-port cable.

Starting up the GUI Software

Once the executable file for the "XRT83SL34/L34 Evaluation Board GUI" Software has been loaded into the "Host" PC, and Evaluation Board has been connected to the PC, via a parallel-port cable, the user can execute the GUI software, by any of the normal "Window '95" means. This can be by "double-clicking" on the "xrt83SL34/L34.exe" filename or icon, or by going through the "START" button.

The XRT83SL34/L34 Evaluation Board GUI Software Start Up Window

Shortly after the user has selected and started up the “XRT83SL34/L34 Evaluation Board GUI Software, the PC monitor should be display the “Start-up” Window, as depicted below in Figure 15.



Figure 15, The “Start-Up” Window, within the XRT83SL34/L34 Evaluation Board GUI Software

Figure 15 indicates that the “Start-Up” Window consists of a menu bar which contains the following three “pull-down” menus:

- File
- Tests
- Help

Each of these “Pull-down” menus will be discussed in some detail below.

The File pull-down Menu

Figure 16 presents an illustration of the “Start-Up” window with the “File” pull-down menu fully visible.

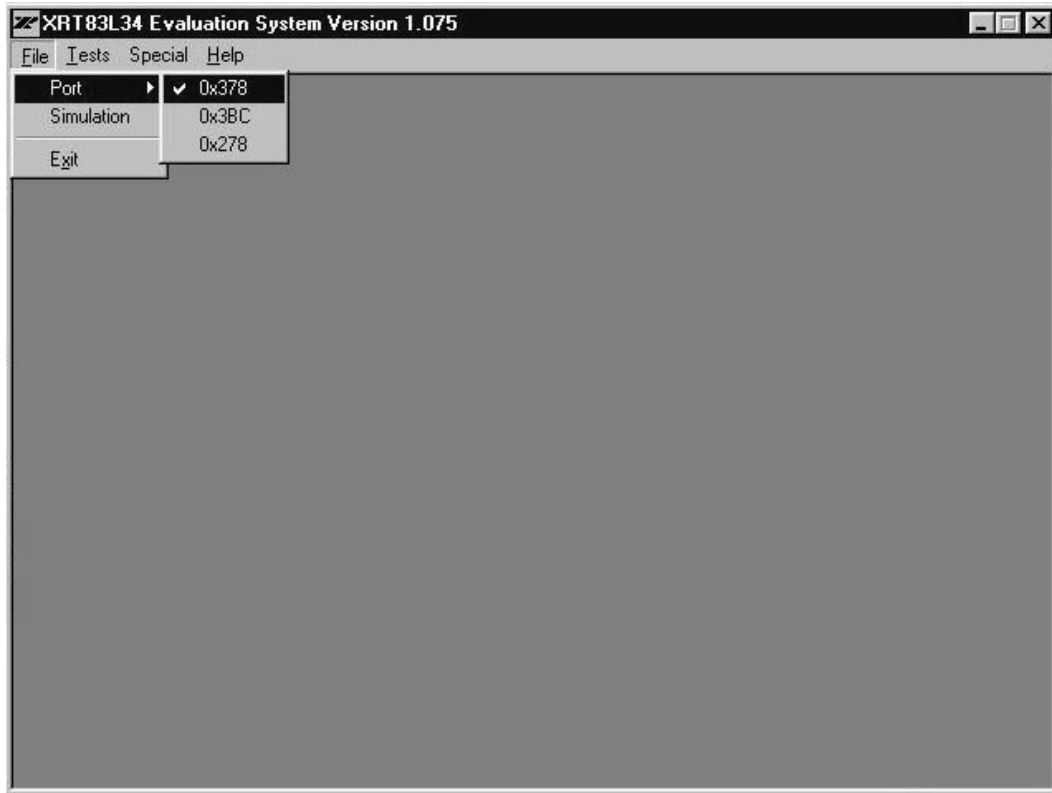


Figure 16, Illustration of the “File” Pull-down Menu

Figure 16 indicates that the “File” pull-down menu contains the following options:

“Port”

“Exit”

Each of these options are discussed in detail below

Port Setup

The “Port Setup” option permits the user to select the address where the parallel port is located. The default address is 0x378. A check mark indicates which address it is currently set to.

Note: This section DOES NOT change your system configurations for the parallel port. This option is needed ONLY when the address to your system’s parallel port is not set at 0x378.

Exit

The “Exit” option permits the user to “gracefully” terminate and exit the program.

The “Tests” pull-down Menu

Figure 17 presents an illustration of the “Start-up” window with the “Tests” pull-down menu fully visible.

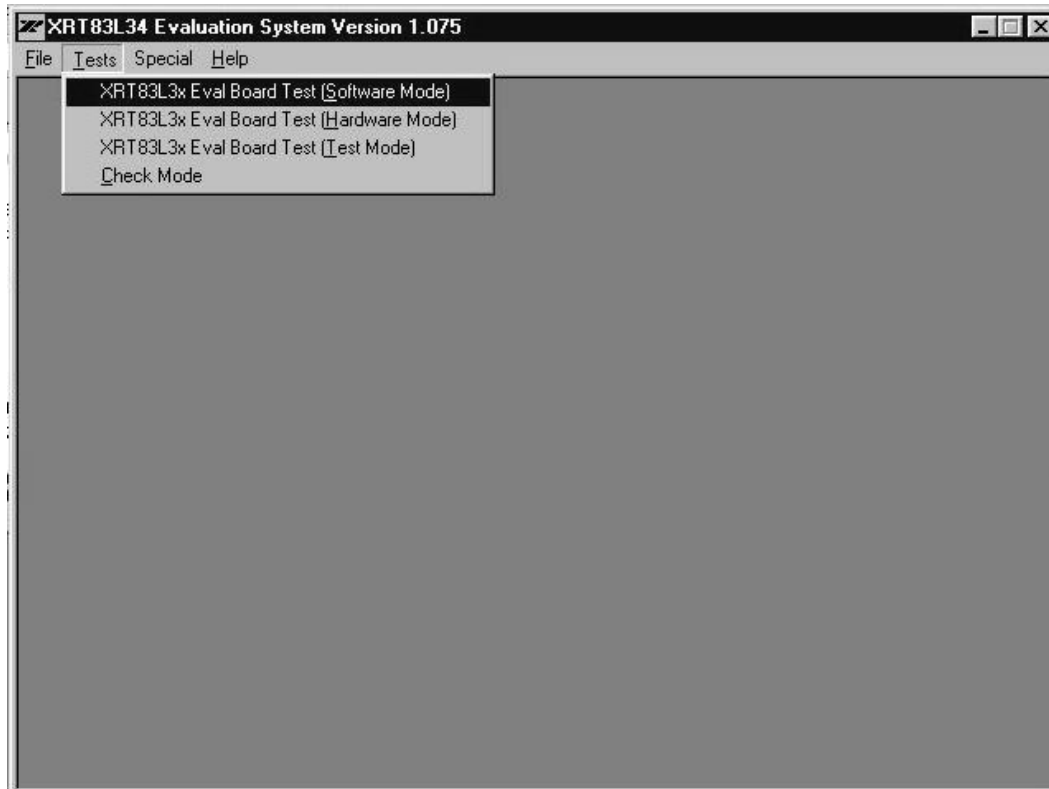


Figure 17, Illustration of the “Tests” Pull-down Menu

Figure 17 indicates that the “Tests” option only consists of the “Evaluation Board Test” option. Once the user selects this option, then the “Host Mode” or “Hardware Mode” Dialog (depending on the board configuration) will appear as illustrated below, see Figure 18 and 19.

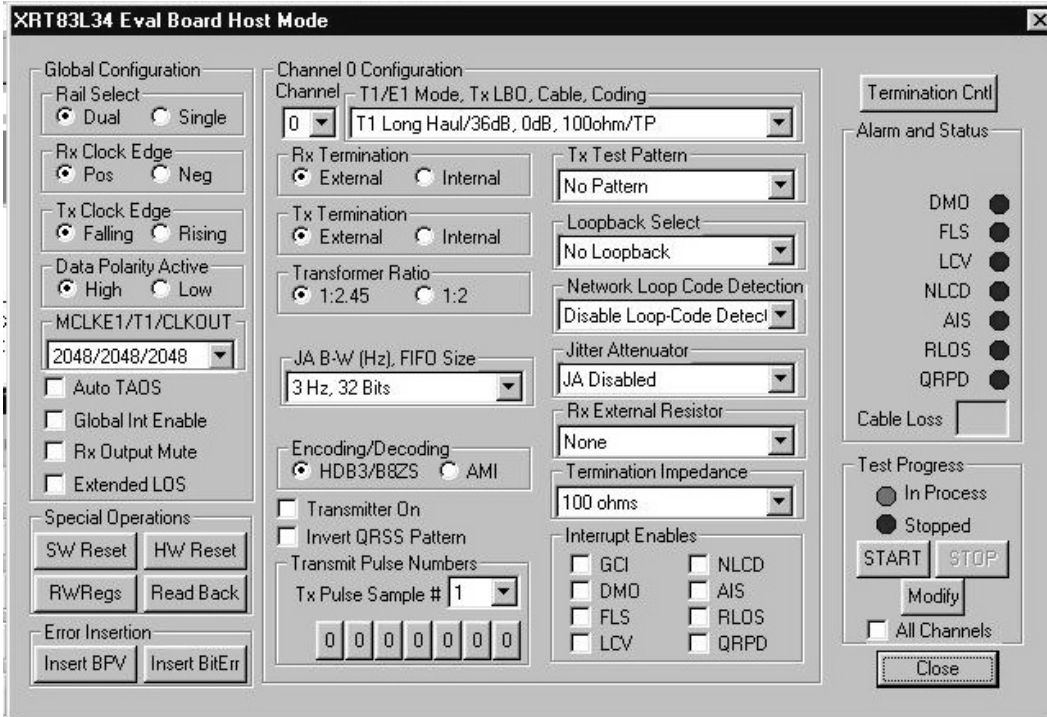


Figure 18, Illustration of Host Mode Test Dialog Box

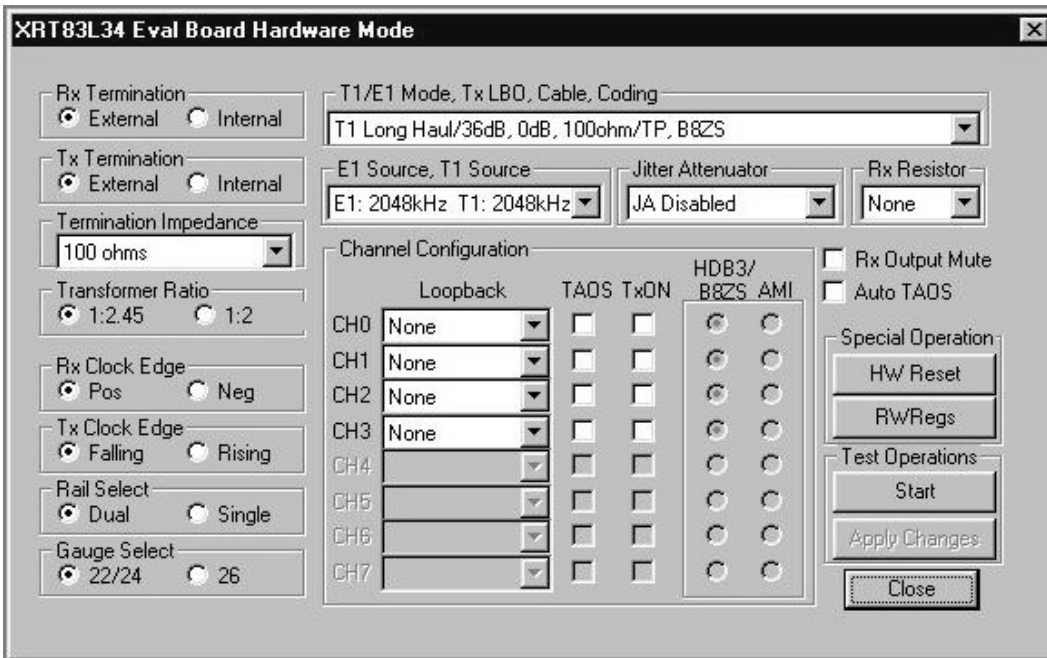


Figure 19, Illustration of Host Mode Test Dialog Box

At this point, the user will be able to specify his/her configuration settings for the XRT83SL34/L34 device; and implement these settings. A more detailed discussion of the “Host Mode” and “Hardware Mode” Dialogs is presented in the next section.

The “Help” pull-down Menu

Figure 20 presents an illustration of the “Start-up” window with the “Help” pull-down menu fully visible.

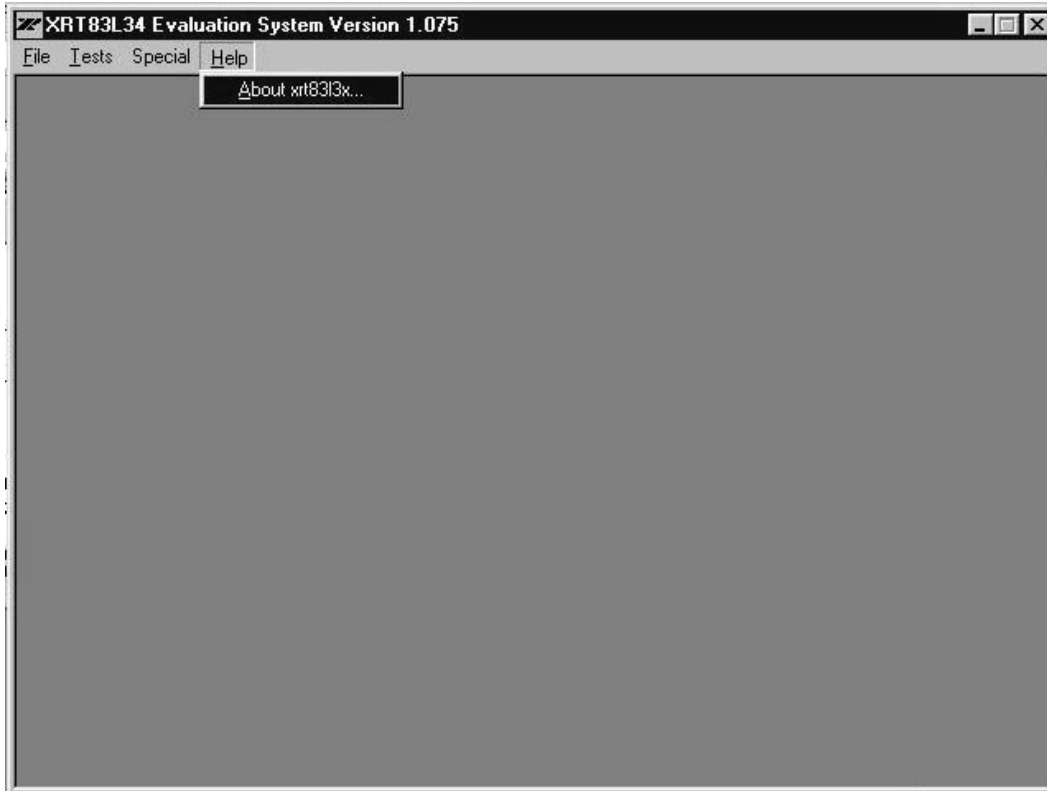


Figure 20, Illustration of the “Help” Pull-down Menu

Figure 20 indicates that the “Help” option consists of two options.

- About XRT83L3x Eval Software

Host Mode Test

Figure 21 presents an illustration of the Host Mode Test Dialog Box. The GUI should display this box under the following condition.

- In response to the selection of the “Evaluation Board Test” option within the “Test” pull-down menu.

The Host Mode Test Dialog Box represents the main interface that the user will have to the XRT83SL34/L34 Evaluation Board, via the GUI Software. All options that are offered by the XRT83SL34/L34 device, when operating in the “Host” Mode, are offered via the “Host Mode Test Dialog Box”. The following sections explain the options and features associated with the Host Mode Test Dialog Box.

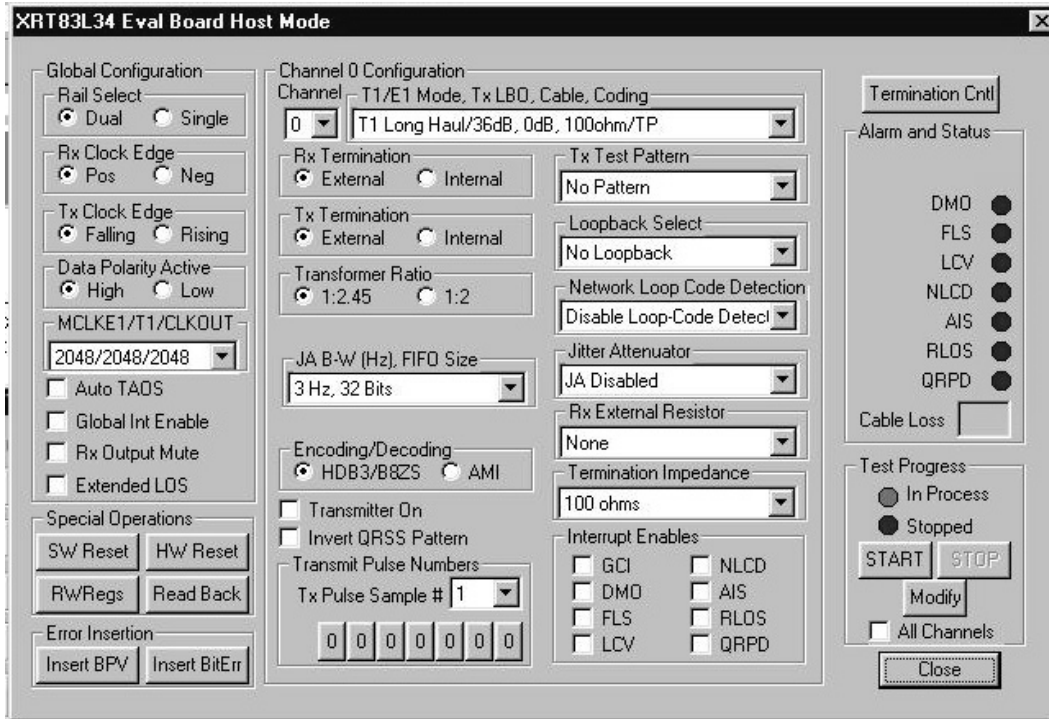


Figure 21, Illustration of the Host Mode Test Dialog Box

Figure 21 indicates that the Host Mode Test Dialog Box consists of the following sections

- Global Configurations
- Channel Configuration (Ch.0, Ch.1, Ch.2, or Ch.3)
- Alarms and Status (Current Channel)
- Special Operations
- Error Insertion (Current Channel)
- Test Progress

Each of these sections is discussed in detail.

The Global Configuration Section

The “Global Configuration” Section of the Host Mode Test Dialog Box permits the user to do the following. It is important to note settings in this section take effect only after either “START” or “Modify” buttons are pressed.

- Rail Select, Select the Rail Select (Data Format) (i.e., Single Rail or Dual Rail)
- Rx Clock Edge, Select which edge of RCLK the output data of all channels is to be updated.
- Tx Clock Edge, Select which edge of TCLK the transmit data of all channels is to be sampled.
- Data Polarity Active, Select Data Polarity Active state to be high or low.
- MCLKE1/T1/CLKOUT, Select MCLKE1/T1/CLKOUT clock sources. A drop list box provides all possible settings. For example the setting 1544/2048/1544 sets the E1 clock source to 1544 MHz, the T1 clock source to 2048 MHz and the master clock rate to 1544 MHz.
- Auto TAOS, Enable/disable Auto TAOS (i.e., Automatic Transmission of All Ones for all channels)
- Global Int Enable, when checked enables interrupt generation for all channels.
- Rx Output Mute, mutes receive outputs of RPOS/RDATA and RNEG/LCV pins to a “0” state for any channel that detects an RLOS condition.
- Extended LOS, when enabled the number of zeros at the receive input of each channel before RLOS is declared to 4096 bits.

The Ch.0 to Ch.3 Channel Configuration Section

- The “(Ch.0, Ch.1, Ch.2, or Ch.3) Channel Options” Section of the Host Mode Test Dialog Box permits the user to do the following. It is important to note settings in this section take effect only after either “START” or “Modify” buttons are pressed and only for the current channel (unless All Channels is checked).
- Rx Termination, selects between the internal and external line termination modes for the receiver.
- Tx Termination, selects between the internal and external line termination modes for the transmitter.
- Transformer Ratio, in external termination mode, this selects the transformer ratio for the transmitter. In internal, the selection has no effect.
- Jitter Attenuator Bandwidth, in E1 mode this setting allows the user to select the Jitter Bandwidth. This setting has no effect for T1 mode.
- FIFO Depth, select the size of FIFO Depth for the current channel.
- Jitter Attenuator, used the place the Jitter Attenuator in Transmit/Receive Path or to disable it.
- Encoding/Decoding, selects en/decoding for current channel. Alternate Mark Inversion or HDB3/B8ZS coding schemes can be selected. Setting active only in single rail mode.
- Transmitter On, checked to turn on the transmit section of the current channel. unchecked to tri-state TTIP and TRING.
- Invert QRSS Pattern, setting inverts the polarity of transmitted QRSS pattern.
- Transmit Pulse Numbers, setting for the magnitude of transmit samples in a given transmit period. The user sets the bits individually. The sample numbers are 7-bits long and the MSB is leftmost.
- Tx Test Pattern, allows the user to choose a transmit test pattern. Choices are Transmit/Detect Quasi-Random Signal, Transmit All Ones, Transmit Network Loop-Up Code, Transmit Network Loop-Down Code, and No Pattern.
- Loopback Select, allows the user to select a loopback mode for the current channel. Choices are No Loopback, Dual Loopback, Analog Loopback, and Digital Loopback.
- Network Loop Code Detection, setting is used to monitor the receive data and set the NLCD bit when “00001” (Loop-Up) or “001” (Loop-down) is detected in the receive data for more than 5 seconds. Automatic Loop-Code detection enables remote loopback activation and looks for a Loop-Up code and once detected looks for a Loop-Down code. Upon Loop-Down, the remote loopback is removed.

- Jitter Attenuator, this selection box allows the user to place the jitter attenuator in either the transmit or receive path or neither.
- Rx External Resistor, setting allows the user to set the external Receive fixed resistor to one of the following values: none, 60 ohms, 52.5 ohms, or 37.5 ohms.
- Termination Impedance, selects (for internal termination mode) the transmit and receive termination impedance.
- Interrupt Enables: GCI: enables channel global interrupt generation. DMO: enables DMO interrupt generation. FLS: enables interrupt generation for when the FIFO limit is within 3 bits. LCV: enables interrupt generation for Line Code Violations. NLCD: enables loop-code detection interrupt generation. AIS: enables Alarm Indication Signal detection interrupt generation. RLOS: enables Loss of Receive Signal interrupt generation. QRPD: enables QRSS pattern detection interrupt generation.

Alarm and Status

- DMO: indicates transmit drive values is detected.
- FLS: indicates that the jitter attenuator read/write FIFO pointers are within +/- 3 bits.
- LCV: indicates that the receiver is currently detecting a Line Code Violation or an excessive number of zeros in the B8zs or HDB3 modes.
- NLCD: indicates reception of a loop-up or loop-down code
- AIS: indicates an All Ones Signal is detected by the receiver.
- RLOS: indicates that the receive input signal is lost.
- QRPD: indicates the receiver is currently in synchronization with QRSS pattern.
- Cable Loss, six bit receive selectiveequalizer setting which is also a binary word that represents the cable attenuation indication within +/-1dB.

Special Operations

- SW Reset: software reset sets the register bits in the microprocessor registers to "0".
- HW reset: hardware reset puts device in reset state.
- RWRegs: allows the user to read/write to any register.
- Readback: displays a window with a list of registers and its current value.

Error Insertion

- Insert BPV: inserts a bipolar violation into the transmitted data stream for the current channel.
- Insert Bit Err: inserts a bit error into the transmitted QRSS pattern of the current channel.

Test Progress

- Start Button: applies all the settings in the Global Configuration section and the Channel Configuration section and begins polling of Alarm and Status indicators.
- Modify Button: applies all the settings in the Global Configuration section and the Channel Configuration section.
- Stop Button: stops polling of Alarm and Status indicators.

Hardware Mode Test

Figure 22 presents an illustration of the Hardware Mode Test Dialog Box. The GUI should display this box under the following condition.

- In response to the selection of the "Evaluation Board Test" option within the "Test" pull-down menu.

The Hardware Mode Test Dialog Box represents the main interface that the user will have to the XRT83SL34/L34 Evaluation Board, via the GUI Software. All options that are offered by the XRT83SL34/L34 device, when operating in the “Hardware” Mode, are offered via the “Hardware Mode Test Dialog Box”. The following sections explain the options and features associated with the Host Mode Test Dialog Box.

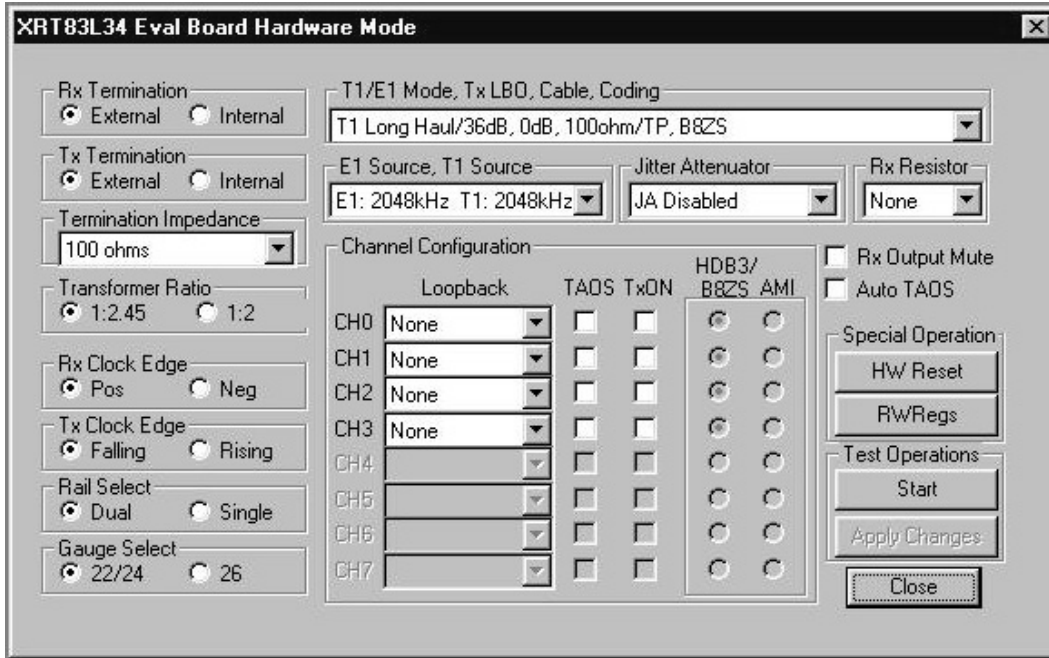


Figure 22, Illustration of the Hardware Mode Test Dialog Box

Figure 22 indicates that the Hardware Mode Test Dialog Box consists of the following

- General Configurations: referring not part of Channel Configurations. It is not specifically labeled as such.
- Channel Configuration (Ch.0, Ch.1, Ch.2, or Ch.3)
- Special Operations
- Test

Each of these is discussed in detail.

General Configuration

The “General Configuration” Section of the Host Mode Test Dialog Box permits the user to do the following. (It is important to note settings in this section take effect only after either “START” or “Apply Changes” buttons are pressed.)

- Rx Termination, selects between the internal and external line termination modes for the receiver.
- Tx Termination, selects between the internal and external line termination modes for the transmitter.
- Termination Impedance, selects (for internal termination mode) the transmit and receive termination impedance.
- Transformer Ratio, in external termination mode, this selects the transformer ratio for the transmitter. In internal, the selection has no effect.
- Rx Clock Edge, Select which edge of RCLK the output data of all channels is to be updated.
- Tx Clock Edge, Select which edge of TCLK the transmit data of all channels is to be sampled.
- Rail Select, Select the Rail Select (Data Format) (i.e., Single Rail or Dual Rail)
- FIFO Depth, select the size of FIFO Depth for the current channel.
- T1/E1 Mode, Tx LBO, Cable, Coding, selects T1/E1, Line Build-Out, Cabling and Coding.
- E1 Source, T1 Source, selects the E1 Source Clock and the T1 Source Clock. When T1 Source is ‘x’ (not present), T1 Source is tied to the E1 Source Clock.
- Jitter Attenuator, used the place the Jitter Attenuator in Transmit/Receive Path or to disable it.
- Rx Resistor, setting allows the user to set the external Receive fixed resistor to one of the following values: none, 60 ohms, 52.5 ohms, or 37.5 ohms.
- Rx Output Mute, mutes receive outputs of RPOS/RDATA and RNEG/LCV pins to a “0” state for any channel that detects an RLOS condition.
- Auto TAOS, Enable/disable Auto TAOS (i.e., Automatic Transmission of All Ones for any channel that the receiver has detected an LOS condition)

The Ch.1 to Ch.8 Channel Configuration

The “(Ch.0, Ch.1, Ch.2, or Ch.3) Channel Options” Section of the Hardware Mode Test Dialog Box permits the user to do the following. (It is important to note settings in this section take effect only after either “START” or “Apply Changes” buttons are pressed and only for the current channel).

- Loopback Select, allows the user to select a loopback mode for the current channel. Choices are No Loopback, Analog Loopback, and Digital Loopback.
- TAOS, enables Transmission of all ones for this channel when RLOS condition is detected.
- TxOn, checked to turn on the transmit section of the current channel. unchecked to tri-state TTIP and TRING.
- HDB3/B8ZS,AMI, selects en/decoding for current channel. Alternate Mark Inversion or HDB3/B8ZS coding schemes can be selected. Setting active only in single rail mode.

Special Operations

- HW reset: hardware reset puts device in reset state.
 - RWRegs: allows the user to read/write to any register.
- Readback: displays a window with a list of registers and its current value.